Refine Search

Search Results -

Term	Documents
(27 AND 29).PGPB,USPT.	0
(L29 AND L27).PGPB,USPT.	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L30

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Monday, June 07, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT; PLUR=YES; OP=ADJ			
L30	L29 and L27	0	L30
L29	comparing near3 search value	33	L29
L28	L27 and (comparing near6 (hash near3 collisions))	0	L28
L27	('6735670' |'6473846' |'6226710')!.PN.	3	L27
L26	L24 and @ad<20010101	19	L26
L25	L24 and ad<20010101	35	L25
L24	L23 and (hash near3 collision)	35	L24
L23	CAM near2 memory	2931	L23
L22	CAM near3 memory	3295	L22
L21	L20 and @ad<20010101	76	L21
L20	L19 near3 L18	113	L20
L19	collision	70848	L19
L18	CAM	215243	L18

L17	6665297.pn. and (hash near3 collision)	1	L17
L16	L15 and hash	1	L16
L15	5390359.pn.	1	L15
L14	5390359.pn. and (hash near3 collision)	1	L14
L13	5390359.pn. and hash	1	L13
L12	530359.pn. and hash	0	L12
L11	L10 and hash	1	L11
L10	6665297.pn.	1	L10
L9	L8 and @ad<20010101	24	L9
L8	search$3 near3 collision near3 hash	64	L8
L7	compar$3 near3 search$3 near3 collision near3 hash	0	L7
L6	L4 and (hash near3 collision)	1	L6
L5	L4 ansd (hash near3 collision)	0	L5
L4	('20030037055')!.PN.	1	L4
L3	L2 and L1	3	L3
L2	09/927599	3	L2
L1	hash near3 collision	468	L1

END OF SEARCH HISTORY

Your search matched **3** of **1043368** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

content <and> addressable <and> memory <and> h Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **Study of an efficient simulation method**
Chang, Y.-R.;
Computers and Digital Techniques, IEE Proceedings- , Volume: 146 , Issue: 5 , Sept. 1999
Pages:253 - 258

[Abstract] [PDF Full-Text (428 KB)] **IEE JNL**

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2 **GaAs VLSI implementation of a 2.5 Gb/s ATM label translator**
Moussa, I.; Lassen, P.S.;
Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1996. Technical D 1996., 18th Annual , 3-6 Nov. 1996
Pages:69 - 72

[Abstract] [PDF Full-Text (520 KB)] **IEEE CNF**

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3 **Looking for analogues in structural safety management through connectionist associative memories**
Lazzari, M.; Salvaneschi, P.; Brembilla, L.;
Neural Networks for Identification, Control, Robotics, and Signal/Image Proce 1996. Proceedings., International Workshop on , 21-23 Aug. 1996
Pages:392 - 400

[Abstract] [PDF Full-Text (476 KB)] **IEEE CNF**

Terms used **content addressable memory** and **hash algorithm** Found **9** of **134,037**

Sort results by: relevance

Display results: expanded form

Save results to a Binder

Search Tips

Open results in a new window

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Results 1 - 9 of 9

Relevance scale

1 An associative file store using fragments for run-time indexing and compression

R. M. Lea, E. J. Schuegraf

June 1980 **Proceedings of the 3rd annual ACM conference on Research and development in information retrieval**

Full text available: pdf(690.98 KB) Additional Information: full citation, references

2 A high performance transparent bridge

Martina Zitterbart, Ahmed N. Tantawy, Dimitrios N. Serpanos

August 1994 **IEEE/ACM Transactions on Networking (TON)**, Volume 2 Issue 4

Full text available: pdf(1.41 MB) Additional Information: full citation, references, index terms

3 A microprogrammed keyword transformation unit for a database computer

Krishnamurthi Kannan, David K. Hsiao, Douglas S. Kerr

October 1977 **Proceedings of the 10th annual workshop on Microprogramming**

Full text available: pdf(706.09 KB) Additional Information: full citation, abstract, references, citings, index terms

The design of a microprogrammable microprocessor-based keyword transformation unit for a database computer(DBC) is described. The DBC, a specialized back-end computer capable of managing 109 - 1010 bytes of data, consists of two loops of memories and processors, the structure loop and the data loop, connected through a database command and control processor (DBCCP). The structure loop is used to retrieve and update the large amount (10

4 LH*—a scalable, distributed data structure

Witold Litwin, Marie-Anna Neimat, Donovan A. Schneider

December 1996 **ACM Transactions on Database Systems (TODS)**, Volume 21 Issue 4

Full text available: pdf(780.63 KB) Additional Information: full citation, abstract, references, citings, index terms, review

We present a scalable distributed data structure called LH*. LH* generalizes Linear Hashing (LH) to distributed RAM and disk files. An LH* file can be created from records with primary keys, or objects with OIDs, provided by any number of distributed and autonomous clients. It does not require a central directory, and grows gracefully, through splits of one bucket at a time, to virtually any number of servers. The number of messages per random insertion is one in general, and three in the w ...

Keywords: algorithms, data structures, distributed access methods, extensible hashing, linear hashing

5 FLATS, a machine for numerical, symbolic and associative computing
Eiichi Goto, Tetsuo Ida, Kei Hiraki, Masayuki Suzuki, Nobuyuki Inada
April 1979 **Proceedings of the 6th annual symposium on Computer architecture**

Functional aspects of a machine called FLATS are described. FLATS aims to efficiently run both numerical and algebraic programs. Overflow free and variable precision arithmetic, table look-up computation, and associative computation based on single-hit content addressed tables are introduced for advanced numerical, algebraic and symbolic computing. Hashing hardware, tag mechanism and hardware list processing are used to realize these features.

6 An associative/parallel processor for partial match retrieval using superimposed codes
Sudhir R. Ahuja, Charles S. Roberts
May 1980 **Proceedings of the 7th annual symposium on Computer Architecture**

This paper presents the design and implementation of special hardware for effective use of the method of superimposed codes. It is shown that the method of superimposed codes is particularly well suited to easy design and implementation of fast and modular hardware. The implementation has shown that a performance gain of two orders of magnitude over conventional software implementations is obtained by using the special hardware. This makes the method of superimposed codes extremely attracti ...

7 A multi-user data flow architecture
F. J. Burkowski
May 1981 **Proceedings of the 8th annual symposium on Computer Architecture**

This paper discusses the design of a prototype data flow machine that has memory management hardware in each memory block. This facility allows loading and deleting code that is produced by independent compilations. The first sections of the paper deal with the general architecture of the machine and the format specifications for the instruction cells, logical addresses, and switch packets. The paper concludes with a discussion of the mapping hardware used in the memory blocks. The results ...

8 Design of a high-performance ATM firewall
Jun Xu, Mukesh Singhal
November 1998 **Proceedings of the 5th ACM conference on Computer and communications security**

9 Trading packet headers for packet processing
Girish P. Chandranmenon, George Varghese
April 1996 **IEEE/ACM Transactions on Networking (TON)**, Volume 4 Issue 2